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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, MINH T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 08/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,061	MANGANARO, GABRIELE	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 9-14 and 17-20 are objected to because of the following informalities:

In claim 9, line 1, "1" should be changed to -- 8 --.

In claims 10-14, the same problem exists as discussed in claim 9.

In claim 17, line 1, "1" should be changed to -- 16 --.

In claims 18-20, the same problem exists as discussed in claim 17.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 7 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 7, the term "base current" recited on line 3 is ambiguous because it is unclear if it is referring to the base of the primary bipolar transistor, or the primary biasing bipolar transistor or the secondary biasing bipolar transistor.

As per claim 14, the same problem exists as noted in claim 7.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-10, 12-17 and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Niknejad et al., article "Fully Integrated Low ...", listed in the IDS, PTO-1449.

As per claim 1, Niknejad discloses a bipolar transistor circuit (Fig. 5) comprising:

a primary bipolar transistor (Q1);

a base resistor (RB1) through which a bias voltage (the voltage at the intersection node of RB1, RB2 and RB4) is applied to the base of the primary bipolar transistor (the voltage at this node provides bias for the base of Q1);

a current source (Q7 and RE7) that drives emitter current (of Q1) through the primary bipolar transistor (Q1); and

a base bias circuit (comprises elements discussed below) generating the bias voltage and comprising:

a current mirror circuit (Q5, Q6, Q7 and Q10) which tracks current through the current source (this fact is the characteristic of a current mirror);

a primary biasing bipolar transistor (Q9) having a β which tracks the β of the primary bipolar transistor and which receives current through the current mirror circuit to develop the bias voltage (the current mirror circuit mirrors the current through Q10. Transistors Q11 and Q12 has the current mirror structure therefore the current at the collector of Q10 is mirrored to the

primary biasing bipolar transistor Q9. In other words, the current through the primary biasing bipolar transistor tracks the current through the current source. By definition, β is the ratio of collector current to base current, the recited limitation the primary biasing bipolar transistor Q9 having a β which tracks the β of the primary bipolar transistor is met); and

a secondary biasing circuit comprising a secondary biasing bipolar transistor (Q12) having a β which tracks the β of the primary bipolar transistor, the secondary biasing bipolar transistor receiving current from the current mirror circuit (as shown, Q10 and Q12 are in series), changes in base current to the secondary biasing bipolar transistor causing changes in current to the primary biasing bipolar transistor (the recited limitation is met by the same reasoning discussed in the previous paragraph).

As per claim 2, the recited bias resistor reads on resistor RB4 connected and function as recited.

As per claim 3, as shown, Q1 and Q9 are NPN.

As per claim 5, Q1 and Q4 constitutes a differential amplifier.

As per claim 6, the circuit shown is a VCO.

As per claim 7, the recited first current mirror reads on Q5-Q7 and Q10, the recited second mirror reads on Q11 and Q12.

As per claim 8, the claim is merely a method to operate the circuit having the structure discussed in claim 1. Since Niknejad teaches the circuit, he inherently teaches the recited method.

As per claims 9-10 and 12-14, these claims are rejected for the same reasons noted in claims 2-3 and 5-7, respectively.

As per claim 15, this claim is rejected for the same reasons noted in claim 1.

As per claim 16, this claim is rejected for the same reasons noted in claim 1. The recited bias resistor reads on RB4.

As per claims 17 and 19-20, these claims are rejected for the same reasons noted in claims 3 and 5-6, respectively.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 11 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Niknejad et al., article "Fully Integrated Low ...", listed in the IDS, PTO-1449.

As per claim 4, Niknejad discloses a circuit as discussed in claim 1 wherein the primary transistors are NPN but he does not explicitly disclose the primary transistors are PNP as called for in the claim.

The examiner takes Official Notice the fact that replacing NPN transistors by PNP transistors in a circuit using bipolar transistors are old and well-known in the art. The examiner further notes that if the applicant challenges such an old and well-known fact, restriction requirement may be proper due to different distinct species, and will be issued later if needed.

It would have been obvious to one skilled in the art at the time of the invention was made to replace the NPN transistors in the Niknejad's circuit by PNP transistors. In situations where

PNP transistors are available but NPN transistors are shorted, one skilled in the art would be clearly motivated to do such a replacement.

As per claims 11 and 18, these claims are rejected for the same reasons and motivation discussed in claim 4.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

8/5/04

Minh Nguyen
Primary Examiner
Art Unit 2816